ABSTRACT

A floor planner tool for integrated circuit design which provides tools and displays for a designer to create a floor plan to define desired placement of circuits defined in a logical netlist by creating a physical hierarchy comprised of nested pblocks. Each pblock is a data structure which contains data which defines which circuits from the logical netlist are assigned to it. Each pblock stands alone and can be input to a place and route tool without the rest of the physical hierarchy. Each pblock data structure contains pointers to the circuits on the netlist assigned to that plbock, identifies other pblocks nested within it and contains a list of pins for the instances within the pblock. Net data structures in the physical hierarchy define which nets are connected to which pins. When pblocks are moved on the floorplan or circuits are moved from one pblock to another, software of the floor planner tool automatically changes the data structures of the physical hierarchy to reflect the new assignments and automatically maintains the same connectivity defined in the logical netlist.

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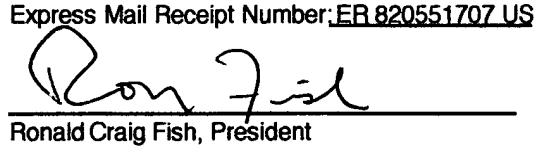

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